UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,218	09/21/2000	Jae-hun Lee	SAM-143	9230

7590 06/30/2004

Mills & Onello LLP
Eleven Beacon Street Suite 605
Boston, MA 02108

EXAMINER	
TRAN, TRANG U	

ART UNIT	PAPER NUMBER
2614	10

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/666,218	Applicant(s) LEE ET AL.	
	Examiner Trang U. Tran	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,8,9,19,20 and 23* is/are rejected.

7)☒ Claim(s) *3-5, 7, 21-22 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed April 16, 2004 have been fully considered but they are not persuasive.

In re pages 10-11, applicants argue that Suemura fails to teach or suggest the present invention as claimed in amended claim 1. In particular, Suemura fails to teach a "transmitter" that "includes a transmitter phase locked loop that, in response to a clock signal, generates a first plurality of non-overlapping clock signals, and for converting the compressed signals to a driving current" (emphasis added), as claimed in amended claim 1...Suemura makes no mention of generating such as "first plurality of non-overlapping clock signals" as claimed in amended claim 1. Nor does Suemura teach or suggest compressing the "skew-compensated signals" in response to the first plurality of non-overlapping clock signals" as claimed in amended claim 1.

In response, the examiner respectfully disagrees. Suemura discloses in column 11, lines 3-59, that "**12 channel parallel digital data at a bit rate per channel of 150 Mb/sec are transmitted, and also skew compensation is realized, a clock converter 42 generates a low frequency clock signal by multiplying the frequency of an input clock signal 35 by 9/8**, parallel digital data 1 covering total of 12 bits are divided into units each of 3 bits, each unit being inputted to each encoders 10, each encoder 10 converts the 3-bit parallel data into 4-bit parallel data through 3B4B encoding, in the encoding, the pattern of "0101" is not used, the parallel data obtained through the encoding are inputted to synchronization pattern adders 11, **in the**

synchronization pattern adders 11, data are written in synchronism to the input clock signal 35 and read out in synchronism to the low frequency clock signal 38" (Fig. 8, col. 11, line 3 to col. 12, line 63). From the above passage, it is clear that the claimed first plurality of non-overlapping clock signals is met by **the input clock signal 35** which inputted the clock signal into parallel synchronization adders (parallel which means non-overlapping clock signal) and the claimed compressing the "skew-compensated signals" in response to the first plurality of non-overlapping clock signals" is met by the **synchronization pattern adders 11, data are written in synchronism to the input clock signal 35 and read out in synchronism to the low frequency clock signal 38**, as recited in the amended claim 1.

In re page 11, applicants argue that, in addition, Suemura fails to teach or suggest "a receiver that includes a receiver phase locked loop that generates a second plurality of non-overlapping clock signals in response to a received clock included in the received optical signal for converting the current signal into a voltage signal, for decompressing the voltage signal in response to the second plurality of non-overlapping clock signals..." (emphasis added), as claimed in amended claim 1... Suemura makes no mention of generating such as "second plurality of non-overlapping clock signals" as claimed in amended claim 1. Nor does Suemura teach or suggest "decompressing the voltage signal in response to the second plurality of non-overlapping clock signals" as claimed in amended claim 1.

In response, the examiner respectfully disagrees. Suemura discloses in column 11, line 35 to column 12, line 30, that "finally, the data are decoded by 4B3B decoding in

decoders 19, meanwhile, **a clock extractor 43 extracts a transmission clock signal 36 from the output of the optical receivers 22**, the transmission clock signal 36 is converted into a low frequency clock signal 38 in a clock frequency divider 45 by dividing the frequency into four, the low frequency clock signal 38 is further converted in a second clock converter 44 into an output clock signal 37 by frequency multiplication by 8/9, **in the decoders 19, data are written in synchronism to the low frequency clock signal 38 and read out in synchronism to the output clock signal 37**". From the above passage, it is clear that the claimed second plurality of non-overlapping clock signals is met by **the low frequency clock signal 38** which inputted the clock signal into parallel decoders 19 (parallel which means non-overlapping clock signal) and the claimed decompressing the voltage signal in response to the second plurality of non-overlapping clock signals" is met by **the decoders 19, data are written in synchronism to the low frequency clock signal 38 and read out in synchronism to the output clock signal 37**, as recited in the amended claim 1.

In re pages 11-12, applicants argue that, with regard to the rejection of independent claim 19, it is submitted that Suemura fails to teach or suggest, a "data restoration and skew compensation unit in the receiver" that includes a "phase locked loop for generating first through n-th non overlapped clock signals, each having a predetermined offset to prevent mutual overlapping" (emphasis added) as claimed in claim 19...there is no teaching or suggestion in Suemura that non-overlapped clock signal are used in this manner in the receiver, nor is there a teaching or suggestion that

a determination of the non-overlapped clock signal "having the greatest timing margin" is made in Suemura.

In response, the examiner respectfully disagrees. As discussed in claim 1 above, Suemura does indeed disclose the claimed limitations a "data restoration and skew compensation unit in the receiver" that includes a "phase locked loop for generating first through n-th non overlapped clock signals, each having a predetermined offset to prevent mutual overlapping". Additionally, Suemura discloses in column 12, line 31 to col. 14, line 8, that "**it will be seen that the synchronization pattern detectors 16, controller 41 and bit rotator 17 realize skew compensation as well as frame synchronization**, Fig. 10 shows the detailed structure example of the synchronization pattern detectors 16, controller 41 and bit rotator 17, actually, the individual circuits are not clearly distinguished from one another, and they fulfill their respective functions collectively, the operations of the circuits will be described in detail with reference to the time chart of Fig. 12". From the above passage, it is clear that Suemura disclose the skew compensation that determination of the non-overlapped clock signal "having the greatest timing margin" as recited in claim 19.

In re pages 12-13, applicants argue that with regard to the rejection of independent claim 23, Suemura fails to teach or suggest all the limitations as discussed in claim 19.

In response, as discussed above, Suemura does indeed disclose all the limitations of claim 19.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 6, 9, 19-20 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Suemura et al (US Patent No. 5,887,039).

In considering claim 1, Suemura et al discloses all the claimed subject matter, note 1) the claimed a video controller for separating color signals and a horizontal/vertical synchronous signal from an original video signal, and for transmitting the color signals and the horizontal/vertical synchronous signal in response to externally-applied predetermined data enable signal and clock signal is met by the parallel digital data 1 which is covering a total of 12 bits are divided into units each of 3 bits, each unit being inputted to each encoder 10 (Figs. 8 and 9, col. 11, lines 3-26), 2) the claimed a transmitter that includes a transmitter phase locked loop that, in response to a clock signal, generates a first plurality of non-overlapping clock signals, the transmitter for skew-compensating and compressing signals received from the video controller and for converting the compressed signals to a driving current is met by the transmitter which includes the encoder 10, the sync pattern adder 11, the input clock signal 42, the timing pulse generator 30 and the P/S converter 12 (Figs. 8 and 9, col.

11, lines 3-32), 3) the claimed a transmission photo diode for converting the driving current to an optical signal and for outputting the optical signal is met by the optical transmitters 20 (Figs. 8 and 9, col. 11, lines 32-35), 4) the claimed an optical transmission line comprised of a predetermined number of channels, for transmitting the optical signal is met by the optical fibers 21 (Figs. 8 and 9, col. 11, lines 32-35), 5) the claimed a reception photo diode for converting the optical signal received from the optical transmission line into a current signal and for outputting the current signal is met by the optical receivers 22 (Figs. 8 and 9, col. 11, lines 35-37), and 6) the claimed a receiver that includes a receiver phase locked loop that generates a second plurality of non-overlapping clock signals in response to a received clock included in the received optical signal for converting the current signal into a voltage signal, for decompressing the voltage signal in response to the second plurality of non-overlapping clock signals, for compensating for the skew of the voltage and for restoring the original signal is met by the receiver side and the decoders 19 (Figs. 8 and 9, col. 11, line 37 to col. 14, line 8).

In considering claim 6, Suemura et al discloses all the claimed subject matter, note 1) the claimed wherein the receiver phase locked loop further generates a clock signal in response to the received clock included in the received optical signal is met by the clock extractor 43 which extracts a transmission clock signal 36 form the output of the optical receiver 22 and the output clock signal 37 (Figs. 8 and 9, col. 11, line 60 to col. 12, line 19), 2) the claimed an optical receiver for converting current signals received from the reception photo diode into voltage signals, and for duty-compensating

and level-converting the voltage signals to obtain digitalized signals which are different channel data is met by the optical receivers 22 (Figs. 8 and 9, col. 11, lines 35-37), 3) the claimed a data restoration and skew compensation unit for receiving channel data that has been compressed by the transmitter, for decompressing the compressed data in response to the plurality of non-overlapping clock signals, and for skew-compensating the decompressed data to obtain different channel data each having a predetermined number of bits is met by the skew compensation which includes the synchronization pattern detectors 16, controller 41 and bit rotator 17 (Fig. 9, col. 12, line 31 to col. 14, line 8), and 4) the claimed a descrambler for descrambling in response to the direct current balance information in each of the channel data, so that the low level and high level of the channel data balance with each other is met by the decoders 19 (Fig. 9, col. 12, line 31 to col. 14, line 8).

In considering claim 9, Suemura et al. discloses all the claimed subject matter, note 1) the claimed a first latch unit for latching for latching received serial data in units of n+N-1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the second plurality of non-overlapping clock signals comprising first through n-th non-overlapped clock signals, and for outputting N n-bit latch state data having the time difference of a predetermined offset therebetween is met by the serial-to-parallel (S/P) converters 18 which convert the serial data into parallel data (Fig. 9, col. 12, lines 31-66), 2) the claimed the second latch unit for latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals is met

by the first register 60 and the second register 61 (Figs. 9-11, col. 12, line 59 to col. 13, line 46), and 3) the claimed a synchronizer for outputting state data from which the synchronous signal is detected, among data latched by the second latch unit, as restored information data, in response to a predetermined synchronous existence signal and the X-th non-overlapped clock signal, each has a predetermined offset so that the clock signals are not overlapped with each other is met by the AND gate 56 which takes a logical AND operation of the synchronization pattern group detection signal Sa and the selector 64 which selects respective one of the ports of the states 0 to 3 (Figs. 9-12, col. 13, line 10 to col. 14, line 8).

In considering claim 19, Suemura et al. discloses all the claimed subject matter, note 1) the claimed a first latch unit for latching for latching received serial data in units of n+N-1 (where N is a positive integer greater than or equal to 3) bits in parallel in response to the first through n-th non-overlapped clock signals, and for outputting N n-bit latch state data having the time difference of a predetermined offset therebetween is met by the serial-to-parallel (S/P) converters 18 which convert the serial data into parallel data (Fig. 9, col. 12, lines 31-66), 2) the claimed the second latch unit for latching in parallel the N state data in response to an X-th ($1 \leq X \leq n$) non-overlapped clock signal having the greatest timing margin among the first through n-th non-overlapped clock signals is met by the first register 60 and the second register 61 (Figs. 9-11, col. 12, line 59 to col. 13, line 46), and 3) the claimed a synchronizer for outputting state data from which the synchronous signal is detected, among data latched by the second latch unit, as restored information data, in response to a predetermined

synchronous existence signal and the X-th non-overlapped clock signal is met by the AND gate 56 which takes a logical AND operation of the synchronization pattern group detection signal Sa and the selector 64 which selects respective one of the ports of the states 0 to 3 (Figs. 9-12, col. 13, line 10 to col. 14, line 8).

In considering claim 20, the claimed wherein the predetermined offset is the width of a unit bit constituting the serial data is met by the serial-to-parallel (S/P) converters 18 which convert the serial data into parallel data (Fig. 9, col. 12, lines 31-66).

Claim 23 is rejected for the same reason as discussed in claim 19.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura et al (US Patent No. 5,887,039).

In considering claim 8, Suemura discloses all the limitations of the instant invention as discussed in claims 1 and 6 above, except for providing the claimed wherein the optical receiver further comprises a power down controller for powering down the bias circuit so that it does not operate, in response to an externally-applied power down control signal. The capability of using the power down controller is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious

to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using power down controller into Suemura's system in order to control the power of the bias circuit.

6. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suemura et al (US Patent No. 5,887,039) in view of Sakamoto et al (US Patent No. 6,557,110 B2).

In considering claim 2, Suemura et al discloses all the claimed subject matter, note 1) the claimed wherein the transmitter phase locked loop further generates a synchronized clock signal to serve as a clock signal for data transmission in response to the externally-applied clock signal is met by the timing pulse generator 40 which generates a timing signal 30, which is "1" during one of 9 time slots and "0" otherwise and is inputted simultaneously to the 4 synchronization pattern adders 11 (Figs. 8 and 9, col. 11, lines 27-35), 2) the claimed a skew compensator for receiving data, each data having a predetermined number of bits, from the video controller; in response to the synchronized clock signal, via different channels, and compensating for a skew which is generated between the channel data in response to the synchronized clock signal is met by the synchronization pattern adders 11 in which the data are written in synchronism to the input clock signal 35 and read out in synchronism to the low frequency clock signal 38 (Figs. 8 and 9, col. 11, lines 3-35), 3) the claimed a data serialization unit for compressing the scrambled channel data in response to the synchronized clock signal to obtain 1-bit channel data is met by the P/S converters 12 (Figs. 8 and 9, col. 11, lines 3-35), and 4) the claimed an optical driver for receiving the

compressed channel data and the clock signal as different channel data and converting the received data into current signals, in order to drive the transmission photo diode is met by the optical transmitters 20 (Figs. 8 and 9, col. 11, lines 32-35).

However, Suemura et al explicitly does not disclose the claimed a scrambler for counting the number of high levels and the number of low levels of each of the skew-compensated channel data, and adding the counted information to each of the channel data to serve as direct current balance information, and transmitting the resultant data.

Sakamoto et al teach that counter circuit 123 begins counting upon receiving a start signal Scs and stops counting upon receiving a reset signal Scr, as illustrated in Figs. 7 and 8, counter circuit 123 outputs reference timing signals Sref at a period to match the frame length, the contents of the shift registers 121 are transferred to data latch 122 at an output timing given by the reference timing signals Sref (Fig. 5, col. 15, line 40 to col. 16, line 35).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the counter as taught by Sakamoto et al into Suemura et al's system in order to provide a channel-to-channel skew compensation apparatus that can prevent outputting erroneous data.

Allowable Subject Matter

7. Claims 3-5, 7, 21-22 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trang U. Tran whose telephone number is (703) 305-0090. The examiner can normally be reached on 8:00 AM - 5:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TT TT
June 26, 2004

MICHAEL H. LEE
PRIMARY EXAMINER